AMENDMENTS TO THE CLAIMS

1-3. (Cancelled)

4. (Currently Amended) A semiconductor memory device comprising:

a volatile latch circuit for holding data;

a nonvolatile ferroelectric capacitor circuit for holding data;

a switch circuit for connecting said latch circuit with said ferroelectric capacitor circuit and disconnecting said latch circuit from said ferroelectric capacitor circuit; and

a logic circuit having a configuration that can be changed in accordance with the data held in said latch circuit;

wherein said switch circuit is operable to connect said latch circuit with said ferroelectric capacitor circuit only when data is transferred between said latch circuit and said ferroelectric capacitor circuit;

~~The semiconductor memory device according to Claim 1, wherein:~~

wherein said ferroelectric capacitor circuit includes

a first circuit having a nonvolatile ferroelectric element for holding data, and

a second circuit having a nonvolatile ferroelectric element for holding data;

and

wherein said switch circuit is operable to select one of said first circuit and said second circuit, and connect the selected circuit with said latch circuit only when data is transferred between said latch circuit and said ferroelectric capacitor circuit.

5-6. (Canceled)

7. (Previously Presented) The semiconductor memory device according to Claim 4, further comprising circuit blocks for processing data,

wherein one of said circuit blocks includes said latch circuit, said ferroelectric capacitor circuit, said switch circuit and said logic circuit, and each of the other circuit blocks has a same structure as said one circuit block.

8. (Currently Amended) The semiconductor memory device according to Claim 7, further comprising a control unit operable to control the reconfiguration of a circuit configuration for each circuit block.

9. (Currently Amended) The semiconductor memory device according to Claim 8, wherein:

said circuit blocks each include a first circuit block and a second circuit block; and

said control unit is operable to reconfigure [[a]] the circuit configuration of said second circuit block while data is processed in said first circuit block.

10. (Currently Amended) The semiconductor memory device according to Claim 8, wherein said control unit is operable to reconfigure [[a]] the circuit configuration of said circuit blocks, each of which is separately reconfigured.

11. (Currently Amended) The semiconductor memory device according to Claim 8, wherein:

said circuit blocks each include circuit block groups corresponding to respective stages

of a pipeline processing; and

said control unit is operable to reconfigure [[a]] the circuit configuration of each circuit block group in order of the stages.

12. (Currently Amended) The semiconductor memory device according to Claim 11, wherein said control unit is operable to make the circuit block groups start processing the respective stages in the order of the reconfiguration.

13. (Original) The semiconductor memory device according to Claim 11, wherein said control unit is operable to sequentially reconfigure said circuit blocks starting from a circuit block on which processing of a stage is completed.

14. (Previously Presented) The semiconductor memory device according to Claim 8, wherein:

the data processing includes repetitive processing, and

said control unit is operable to reconfigure one of said circuit blocks so as to feed back to said one of said circuit blocks with a processing result before a first iteration, and to reconfigure said one of said circuit blocks so as not to feed back to said one of said circuit blocks just before a last iteration.

15-29. (Canceled)